AF

IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

INVENTORS:

Thomas J. Krutsick

CASE: 5

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TITLE: FIELD PLATED RESISTOR WITH ENHANCED ROUTING AREA THEREOVER

SERIAL NO. 09/650,604

GROUP ART UNIT 2826

FILING DATE 04/18/00

EXAMINER AHMED N. SEFER

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313-1450

SIR:

Please find enclosed an Appeal Brief, in triplicate, for the matter identified above. This is a revised version of the Appeal Brief filed October 12, 2004. The Examiner objected to the form of the brief. The version enclosed with this cover letter attempts to respond to the Examiner's objections.

Respectfully submitted,

Peter V.D. Wilde
Reg. No. 19658

Date: JAN 05 2005

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BRIEF ON APPEAL

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated 04/26/04 finally rejecting claims 28-30 and 32-41. Claim 42 is objected to for formal reasons and is retained as pending but not appealed.

Claims 28-30 and 32-41 are the claims on appeal. No claim stands allowed.

Real party in interest – 37 C.F.R. 41.37(i)

The real party in interest is in the caption to this brief. The Assignee of record of the entire interest in the application is Lucent Technologies Inc. By subsequent Assignment from Lucent Technologies Inc. to Agere Systems Inc., the current owner of the entire interest is Agere Systems Inc.

Related appeals and interferences – 37 C.F.R. 41.37 (ii)

None known.

Status of claims - 37 C.F.R. 41.37 (iii)

Claims 28-30 and 32-41 stand rejected and are submitted for consideration in this appeal. In applicant's response dated February 3, 2003, claim 31 was canceled. It was inadvertently included as a claim on appeal in the Notice of Appeal.

A correct copy of claims 28-30 and 32-41 is appended to this brief as APPENDIX A.

Status of Amendments - 37 C.F.R. 41.37 (iv)

All amendments filed have apparently been entered.

Summary of claimed subject matter - 37 C.F.R. 41.37 (v)

The description of the method for producing the device of the claimed

invention involves many steps, and the steps are described in many figures. To simplify the summary of the invention, the following is provided to aid in mapping the claimed elements from the main independent claim, claim 28, to the structural features shown in the drawing. As will become evident, to do this most effectively requires that more than one figure be referenced. To avoid confusion due to possible line number changes as the result of the amendments to the specification made in the amendment filed June 10, 2001, the references to the specification are to the specification as originally filed. (The amendments to the specification were made before the new amendment practice and therefore there are no amended pages that are complete with new reference numbers.)

28. An integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. a resistor body **(38 in Fig. 7)** formed in a semiconductor substrate **(20 in Fig. 7)**, the resistor body having first **(46 in Fig. 7)** and second **(56 in Fig. 12)** contact regions,

b. a first insulating layer **(40 in Fig. 7)** on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface,

c. a contact window **(44 in Fig. 6)** in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. a field plate **(50 in Fig. 7)** on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region **(46 in Fig. 7)** of the resistor,

e. a second insulating layer **(66 in Fig. 16)**, with a first portion of the second insulating layer at least substantially covering the field plate **(50 in Fig. 13)**,

f. an electrical contact **(82 in Fig. 16)** to the top surface of the field plate,

g. an electrical contact **(84 in Fig. 16)** to the second contact region of the resistor, and electrically insulated from the field plate, and

h. a plurality of metal conductors **(90 in Fig. 16)** formed on the first portion of the second insulating layer.

The effect of the structure claimed above is that the metal conductors 90 **(Fig. 16, specification page 9, lines 11-19)** are electrically shielded from the resistor body 38 **(Fig. 7, specification page 5, lines 5-10, page 9, lines 18-23, page 10, lines 1-3)** due to the intervening field plate 50 **(Fig. 13, specification page 6, lines 12-19)**. In the absence of field plate 50, signals in the metal conductors would couple to the resistor body in substrate 20 **(Fig. 7,**

specification page 4, lines 4,5), causing unwanted capacitive coupling. Due to the unwanted capacitive coupling, the area over the resistor body is normally a prohibited area for electrical surface conductors, like those designated 90. That means, without the field plate, those metal conductors would need to be routed elsewhere, thus consuming valuable chip area.

The concept of valuable chip area is central to the invention.

According to a main feature of the invention, valuable chip area is further conserved by locating one of the contacts to the resistor body 38 in the same area as the field plate. Thus the first contact goes through the field plate to contact the resistor body underneath the field plate, at region 46 **(Fig. 7, specification page 5, lines 20-23, page 6, lines 3-5)**. Note that the second contact region, at 56 **(Fig. 12, specification page 7, lines 21-23, page 8, lines 19-21)**, is located outside of the field plate area. That would be the normal and obvious place to put the second contact, as well as the first contact. But in locating the first contact in the area of the field plate, valuable chip area is saved.

It is worth noting at this point that the contact to the field plate (as well as to resistor body 38), i.e. limitation f.(f. an electrical contact 82 to the top surface of the field plate) can be made to any place on the top surface of the field plate **(Fig. 16, specification page 9, lines 11-14)** . In Fig. 16, the electrical contact 82 is made at the same position as the first contact (46) to the resistor body. That allows a processing economy known in the art, i.e. the use of the same lithography mask to form the two contacts. That is one of the aims

of claims 40-42. However, the contact can be made elsewhere if desired. Accordingly, applicant seeks the somewhat broader invention claimed in claim 28, for example, where the location of the field plate contact is not specific.

References

The primary reference relied on by the Examiner in the final rejection of record is:

Kondo	U.S. Patent No. 4,609,935

The secondary references are:

Nelson et al.	U.S. Patent No. 3,683,491
Davis et al.	U.S. Patent No. 5,200,733

Grounds of rejections to be reviewed on appeal – 37 C.F.R. 41.37 (vi)

Rejections

Claims 40 and 41 stand rejected under 35 U.S.C. 112 as indefinite since the preambles of these claims do not suitably refer to the claim on which they are dependent. This is easily overcome by a simple amendment that will be presented at an appropriate time.

Claims 28-30, and 33-38 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kondo in view of Nelson et al.

Claims 32 and 39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Nelson et al., further in view of Davis et al.

Argument - 37 C.F.R. 41.37 (vii)

35 U.S.C. 112 Rejection

As noted above, this rejection is easily overcome, and applicant certifies that suitable amendments will be made. The error was raised in the final rejection. Applicant chose to make no amendments after the final rejection for procedural reasons.

Claims 28-30, and 33-38 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kondo in view of Nelson et al.

In every substantive rejection in this prosecution, five in all, the Kondo patent was the main reference relied on. The Kondo patent teaches a substrate resistor, a field plate over the resistor, and metal conductors over the field plate. Fig. 1B of Kondo shows the structure clearly. The resistor is shown at 2, and the overlying field plate at 7. Contact 20 is the contact for the field plate. The focus here should be on the contacts to the resistor body 2. Both of the contacts, 4-1 and 4-2, are displaced to either side of the field plate. The chip area consumed to implement the field plate in this structure includes the area of the field plate, plus the area of the first resistor contact 4-1, plus the area of the second resistor contact 4-2.

By contrast, in applicant's claimed field plate implementation, the chip area consumed is the area of the field plate, plus the area of the second resistor contact 82. The first resistor contact 46 does not add to the chip area consumed since it resides below the field plate itself.

Evidently recognizing this absent feature in the Kondo patent, the Examiner combines the Kondo patent with the Nelson et al. patent. Applicant argues, and has argued, that the combination of these two references is inherently flawed. The issue here is not whether parts of the structures of the two prior patents *can* be pieced together to produce the claimed structure, the issue is whether it would be *obvious*, absent applicant's disclosure, to do that. So far, the record does not address the obviousness issue, at least in the context that applicant has argued.

The device described by Nelson et al. is a pinch-off resistor. The reason for incorporating element 41 in the Nelson et al. patent is to achieve the pinch-off function. Absent the need for a pinch-off function, which is the case for both the device of Kondo and the device of applicants, the inclusion of a pinch-off element would be useless and clearly not obvious. There is simply no rational basis for combining these references. The Kondo patent says nothing whatever about pinch-off resistors. And the Nelson et al. patent has nothing to do with field-plated resistors. The mere existence of a contact between an MOS gate electrode and a substrate, as in Nelson et al., is meaningless in the context of applicants' invention. Such contact structures are notorious in the MOS art. The field plate in a field-plated resistor is not an MOS element. Recognizing that in an MOS device (Nelson et al.) there is a deliberate and necessary interaction between a gate electrode (the M element of MOS) over the surface of the semiconductor substrate (the S element of MOS). But that interaction is the direct opposite of the purpose of the field plate in the Kondo invention and in

applicant's invention. A field effect between upper electrodes (6 in Kondo's Fig. 1B and 90 in applicant's Fig. 16) and the semiconductor substrate is what the field plate (7 in Kondo's Fig. 1B and 50 in applicant's Fig. 7) is designed to prevent.

Accordingly, there is no correspondence between element 41 in the Nelson et al. patent, and the field plates in either the Kondo resistor or in applicant's resistor. As described by Nelson et al., and shown in Fig. 9 of their patent, the MOS gate element 41 is intended to form a depletion layer 52 in the substrate of the device. The depletion layer is an MOS element specific to pinch-off transistors. It is not an element of a standard silicon resistor, as described by Kondo or by applicant. Kondo teaches how to prevent Nelson et al's field effect from happening. Why would one combine these teachings?

Moreover, if the structure shown in Fig. 9 of Nelson et al. were to be incorporated in place of elements 4-1, 4-2, and 7 of the Kondo structure, the resulting device would not work. That is because the structure of Nelson et al. produces an MOS depletion layer, and the MOS depletion layer would convert the simple resistor of Kondo into a variable pinch-off resistor. That result, a pinch-off resistor rather than a standard resistor, is not something either Kondo or applicant seeks.

In the final rejection, the Examiner's rationale for citing this combination of references is stated simply as "it would have been obvious to one skilled in the art at the time the invention was made to incorporate Nelson's teachings with Kondo's device, since that would provide high values of resistance."

If the rationale for the combination is to obtain "high values of resistance" the Kondo patent does not appear to mention that as a goal, nor does applicant. Some device applications may require a relatively low value of resistance.

In applicant's response filed December 10, 2003, the argument as substantially set forth above was presented for the Examiner's consideration. The Examiner's response, on page 2 of the final rejection, was:

> "In this case, what Kondo lacks namely, a portion of a bottom surface of a field plate 46 with a portion of a bottom surface extending through a contact window, is disclosed by Nelson in Fig. 9 wherein a field plate 46 with a portion of a bottom surface extending through a contact window in an insulating layer 32 and into contact with a contact region 38 of a resistor 34."

This addresses "how" the references are combined to anticipate the claimed structure but not "why". If it is only necessary, for finding patent merit lacking, to assemble mechanical structures without regard to a rationale basis for the assembly, then finding patentable inventions would be a very rare event. In the instant case, modifying Kondo's device in the manner suggested by the Examiner is not simply a matter of substituting an electrical contact, it converts the simple resistor of Kondo, to another kind of device.

Claims 32 and 39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Nelson et al., further in view of Davis et al.

Claims 32 and 39 add the element of an insulating spacer. The Davis et al. patent is cited as showing this feature. However, applicant relies on the patentable merits of the insulating spacer in combination with the features of claim 28 and 29 (for claim 32) and 35-38 (for claim 39 to support patentability.

Copy of appealed claims 37 C.F.R. 41.37 (viii) – Appended as Appendix A

Conclusion

For the reasons given, applicants' claims 28-30 and 32-39 are believed to be patentable, and the Board is urged to reverse the Examiner's rejection of those claims.

Respectfully submitted,

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APPENDIX A

28. An integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. a resistor body formed in a semiconductor substrate, the resistor body having first and second contact regions,

b. a first insulating layer on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface,

c. a contact window in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. a field plate on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,

e. a second insulating layer, with a first portion of the second insulating layer at least substantially covering the field plate,

f. an electrical contact to the top surface of the field plate,

g. an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate, and

h. a plurality of metal conductors formed on the first portion of the second insulating layer.

29. The integrated circuit of claim 28 wherein the field plate comprises polysilicon.

30. The integrated circuit of claim 29 wherein the first and second insulating layers are SiO_2.

32. The integrated circuit of claim 29 further comprising an insulative spacer formed around the field plate.

33. The integrated circuit of claim 29 wherein the electrical contact to the top surface of the field plate comprises a barrier layer.

34. The integrated circuit of claim 33 wherein the electrical contact to the second contact region of the resistor comprises a barrier layer.

35. An integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. a resistor body formed in a semiconductor substrate, the resistor body having first and second contact regions,

b. a first insulating layer on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface,

c. a contact window in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. a field plate on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,

e. a second insulating layer, with a first portion of the second insulating layer at least substantially covering the field plate,

f. a metal layer comprising

i. an electrical contact to the top surface of the field plate,

ii. an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate, and

iii. a plurality of metal conductors formed on the first portion of the second insulating layer.

36. A method for the manufacture of an integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. forming a resistor body in a semiconductor substrate, the resistor body having first and second contact regions,

b. a first insulating layer on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface,

c. forming a contact window in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. forming a field plate on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,

e. depositing a second insulating layer, with a first portion of the second insulating layer at least substantially covering the field plate,

f. depositing a metal layer,

g. patterning the metal layer to form

i. an electrical contact to the top surface of the field plate,

ii. an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate, and

iii. a plurality of metal conductors formed on the first portion of the second insulating layer.

37. The method of claim 36 wherein the field plate comprises polysilicon.

38. The method of claim 37 wherein the first and second insulating layers are SiO_2.

39. The method of claim 38 further including the step of forming an insulative spacer formed around the field plate.

40. The method of claim 28 wherein the electrical contact to the top surface of the field plate overlies the portion of the bottom surface of the field plate that extends through the contact window in the first insulating layer and into contact with the first contact region of the resistor.

41. The method of claim 35 wherein the electrical contact to the top surface of the field plate overlies the portion of the bottom surface of the field plate that extends through the contact window in the first insulating layer and into contact with the first contact region of the resistor.